WHAT IS CLAIMED IS:

1. An upconverter for modulating an input signal to provide an output signal having a higher frequency than said input signal than the input signal, comprising:

a mixer; and

an amplifier coupled to the mixer, including a plurality of transistors and having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal of a predetermined level, wherein the DC power control signal turns off the transistors of the amplifier when the predetermined level is between approximately -1 to -2 volts.

2. The upconverter as claimed in claim 1 further comprising a source degenerating inductor circuit including a first inductor in parallel with a second inductor and a third inductor, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

3. The upconverter as claimed in claim 1 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

4. The upconverter as claimed in claim 3, wherein the DC bias network comprises a first resistor, a second resistor, a third resistor, and a fourth resistor, the first resistor and third resistor receiving a differential local oscillator signal and the first resistor being in parallel with each of the second resistor, the third resistor, and the fourth resistor.

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5. The upconverter as claimed in claim 1 further comprising a plurality of serially connected diodes coupled to the first input terminal of the amplifier for electro-static discharge protection.

6. The upconverter as claimed in claim 5, wherein the plurality of serially connected diodes comprises a plurality of diode-connected transistors.

7. An upconverter for modulating an input signal to provide an output signal having a higher frequency than the input signal, comprising:

a mixer; and

an amplifier, coupled to the mixer, including matched first and second MESFETs, each MESFET having source, gate, and drain terminals, wherein the gate of the first MESFET receives the input signal, and the gate of the second MESFET is coupled to a DC control voltage capable of turning off the first and second MESFETs.

8. The upconverter as claimed in claim 7 further comprising a plurality of diode-connected MESFETs to protect the upconverter from electro-static discharge.

9. The upconverter as claimed in claim 7 further comprising a source degenerating inductor circuit coupled to the amplifier to reduce noise.

10. The upconverter as claimed in claim 9, wherein the source degenerating inductor circuit comprises a first inductor coupled in parallel with a second inductor and a third inductor.

11. The upconverter as claimed in claim 10, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

12. The upconverter as claimed in claim 7 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

13. An upconverter for modulating an input signal to provide an output signal having a higher frequency, the input signal including an image signal, comprising:

a mixer;

an amplifier, coupled to the mixer circuit, including

a first input terminal for receiving the input signal,

a second input terminal coupled to ground, and

a filter for rejecting noise signals having a same frequency as the image signal of the input signal; and

a first resistor having a first end coupled to the first input terminal of the amplifier and a second end coupled to ground.

14. The upconverter as claimed in claim 13, wherein the filter comprises a second resistor having a same resistance as the first resistor.

15. The upconverter as claimed in claim 13, wherein the filter comprises a resistor in parallel with a serial capacitor and inductor pair.

16. The upconverter as claimed in claim 13, wherein the amplifier comprises matched first and second MESFETs, each MESFET having source, gate, and drain terminals, wherein the gate of the first MESFET receives the input signal and is coupled to one end of the filter, and the gate of the second MESFET is coupled to ground and a second end of the filter.

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17. The upconverter as claimed in claim 16, wherein the mixer comprises matched third and fourth MESFETs, each having source, gate and drain terminals, and matched fifth and sixth MESFETs, each having source, gate and drain terminals,

wherein the sources of the third and fourth MESFETs are coupled to the drain of the first MESFET and the sources of the fifth and sixth MESFETs are coupled to the drain of the second MESFET, the gate of the third MESFET is coupled to the gate of the sixth MESFET and the gate of the fourth MESFET is coupled to the gate of the fifth MESFET, the gates of the third and fourth MESFETs receive a differential local oscillator signal, the drain of the third MESFET is coupled to the drain of the fifth MESFET and the drain of the fourth MESFET is coupled to the drain of the sixth MESFET, and the drains of the third and fourth MESFETs providing an IF output signal.

18. The upconverter as claimed in claim 13 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

19. The upconverter as claimed in claim 13 further comprising a plurality of diode-connected MESFETs to protect the upconverter from electro-static discharge.

20. An upconverter for modulating an input signal to provide an output signal having a higher frequency than the input signal, comprising:

a mixer;

an amplifier, coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal; and

a source degenerating inductor circuit coupled to the amplifier to reduce image noise.

21. The upconverter as claimed in claim 20, wherein the DC control voltage coupled to the second terminal of the mixer turns off the amplifier when the DC control voltage is at a predetermined voltage level.

22. The upconverter as claimed in claim 21, wherein the predetermined voltage level of the DC power control signal is between approximately -1 to -2 volts.

23. The upconverter as claimed in claim 20, wherein the source degenerating inductor circuit comprises a first inductor in parallel with a second inductor and a third inductor.

24. The upconverter as claimed in claim 23, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

25. The upconverter as claimed in claim 20 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

26. The upconverter as claimed in claim 25, wherein the DC bias network comprises a first resistor, a second resistor, a third resistor, and a fourth resistor, the first resistor and third resistor receiving a differential local oscillator signal and the first resistor being in parallel with the second resistor, the third resistor, and the fourth resistor.

27. The upconverter as claimed in claim 20 further comprising a plurality of serially connected diodes coupled to the first input terminal of the amplifier to protect the upconverter from electro-static discharge.

28. The upconverter as claimed in claim 27, wherein the plurality of serially connected diodes comprise a plurality of diode-connected MESFETs.

29. An upconverter for modulating an input signal to provide an output signal having a higher frequency, comprising:

a mixer;

an amplifier, coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal; and

a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier and a resistive network coupled to the amplifier.

30. The upconverter as claimed in claim 29, wherein the DC bias network comprises a first resistor, a second resistor, a third resistor, and a fourth resistor, the first resistor and third resistor receiving a differential local oscillator signal and the first resistor being in parallel with the second resistor, the third resistor, and the fourth resistor.

31. An upconverter for modulating an input signal to provide an output signal having a higher frequency, comprising:

a mixer;

an amplifier, coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal; and

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a plurality of serially connected diode-connected MESFETs coupled to the first input terminal of the amplifier for prevention of electro-static discharge.

32. An upconverter for mixing a single-ended RF signal with a differential local oscillator signal to generate a differential IF signal, comprising:

a source degenerated first differential pair comprising matched first and second transistors, each having source, gate and drain terminals, wherein the gate of the first transistor receives the input signal and the gate of the second transistor receives a ground potential; and

a second differential pair comprising matched third and fourth transistors, each having source, gate and drain terminals, and a third differential pair comprising matched fifth and sixth transistors, each having source, gate and drain terminals,

wherein the sources of the third and fourth transistors are coupled to the drain of the first transistor and the sources of the fifth and sixth transistors are coupled to the drain of the second transistor, the gate of the third transistor is coupled to the gate of the fifth transistor and the gate of the fourth transistor is coupled to the gate of the sixth transistor, the drain of the third transistor is coupled to the drain of the sixth transistor and the drain of the fourth transistor is coupled to the drain of the fifth transistor, the gates of the third and fourth transistors receive the differential local oscillator signal, the drains of the third and fourth transistors supply the differential IF signal, the gate of the first transistor is coupled to the single-ended RF signal, and the gate of the second transistor is coupled to a DC control signal.

33. The upconverter as claimed in claim 32, wherein the DC control voltage

coupled to the gate of the second transistor turns off the first and second transistors when the DC control voltage is at a predetermined voltage level.

34. The upconverter as claimed in claim 32 further comprising a source degenerating inductor circuit coupled to the sources of the first and second transistors to reduce noise, the source degenerating inductor circuit including a first inductor coupled in parallel with a second inductor and a third inductor.

35. The upconverter as claimed in claim 34, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

36. An upconverter chip, comprising:

a semiconductor packaging including a plurality of pins;

a leadframe disposed over the packaging; and

a semiconductor die containing an upconverter disposed over the leadframe, wherein the plurality of pins include a plurality of ground pins, each of the plurality of ground pins coupled to the leadframe to substantially eliminate noise coupled from an external resonator.

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